Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A code processing circuit comprising:

a plurality of coders which encode ~~different kinds of data~~ red data, green data and blue data, respectively;

a first buffer which stores the codes outputted from the coders provided corresponding to said plurality of coders;

a second buffer which stores the lengths of the codes outputted from the coders provided corresponding to said plurality of coders;

a first adder which adds the code lengths stored in the second buffer provided corresponding to said plurality of coders;

a second adder which adds all the code lengths added in the first adder; and

an adjustment unit which adjusts an output code by the unit of 1 bit based on the codes stored in the first buffer, the code lengths stored in the second buffer and the code lengths added in the second adder, the output code being encoded red data, encoded green data and encoded blue data which are continuously output by the unit of 1 byte.

2. (Currently Amended) The code processing circuit according to claim 1, wherein the adjustment unit comprises a code length memory which stores the unit of the output code length; a code length comparator which compares the code lengths added in the second adder with the code lengths stored in the code length memory; an enable signal generator which generates said plurality of different kinds of effective code signals based on the code lengths stored in the second ~~memory~~ buffer and the comparison result of the code length comparator; and an output code generator which generates output codes by the unit of 1 bit from the codes stored in the first ~~memory~~ buffer and the effective code signals generated by the enable signal generator.

3. (Currently Amended) The code processing circuit according to claim 1, further comprising a ratio unit which calculates the ratio of the codes outputted from said plurality of ~~kind of data~~ coders based on an amount of the red data, the green data and the

blue data, wherein the adjustment unit cuts off the codes based on the ratio, when the value of the code lengths added in the second adder is larger than the output unit stored in the code length memory and wherein the cut-off amount of the codes for the red data, the green data and the blue data is in accordance with the ratio.

4. (Original) The code processing circuit according to claim 3, wherein the ratio unit has a ratio calculator which calculates the ratio of each code length according to the code lengths added in the first adder and the code lengths added in the second adder.

5. (Original) The code processing circuit according to claim 3, wherein the ratio unit has a ratio setting unit which previously sets the ratio of each code length added in the first adder.

6. (Currently Amended) The code processing circuit according to claim 4, wherein the ratio unit has a ratio setting unit which previously sets the ratio of each code length added in the first adder, and a switching unit which switches and outputs one of the ratio set in the ratio setting unit and the ratio calculated by the ratio calculator.

7. (Cancelled).

8. (New) The code processing circuit according to claim 6, wherein the ratio unit has a use ratio selector for providing a predetermined use ratio value to the switching unit, wherein the adjustment unit has an enable signal generator which generates said plurality of different kinds of effective code signals based in part on the code lengths stored in the second buffer and based in part on the one ratio output by the switching unit, and wherein the adjustment unit further has an output code generator which generates output codes by the unit of 1 bit from the codes stored in the first buffer and the effective code signals generated by the enable signal generator.